REMARKS

This Amendment is in response to the Office Action mailed on January 4, 2007. Claim 1 is amended editorially to include the features of claim 6. Claim 1 is further amended editorially to reorder the features of claim 1 to support the added features of claim 6. Claim 6 is cancelled without prejudice or disclaimer. No new matter is added. Claims 1 and 3-5 are pending.

103(a) Rejections:

Claims 1, 3, 6 are rejected as being unpatentable over Morikawa (US Patent No. 5,091,818) in view of Yoshimizu (US Patent No. 5,451,814). This rejection is traversed.

Claim 1 is directed to an electronic apparatus that requires, among other features, a first IC comprising a first voltage input terminal and a voltage limiting means that are electrically connected, and a second IC comprising a second voltage input terminal. Claim 1 also requires an external power terminal and a resistor electrically connected at one end to the external power terminal and at the other end to both the first voltage input terminal and the second voltage input terminal. Thus, the resistor and the voltage limiting means limit the input voltage applied to both the first and second voltage input terminals.

The combination of Morikawa and Yoshimizu does not teach or suggest these features. Morikawa is directed to an overvoltage protecting circuit. The rejection correctly notes that Morikawa does not disclose a second IC having a second voltage input terminal. Accordingly, Morikawa also does not disclose a resistor connected at one end to both a first voltage input terminal and a second voltage input terminal.

Yoshimizu does not overcome these deficiencies. Yoshimizu is directed to a multi-chip module integrated circuit that has two IC chips (21, 22) connected directly to an input voltage (VCC) by a bounding wire (37) (see Figure 2b). However, nowhere does Yoshimizu teach or suggest a resistor connected at one end to an external power terminal and at the other end to both a first voltage input terminal and a second voltage input terminal. Thus, Yoshimizu also does not teach or suggest a resistor and a voltage means limiting the input voltage applied to the first and second voltage input terminals. For at least these reasons claim 1 is not suggested by the combination of Morikawa and

Yoshimizu. Claim 3 depends from claim 1 and should be allowed for at least the same reasons.

Claim 4 is rejected as being unpatentable over Morikawa in view of Yoshimizu and further in view of Kawamoto (US Patent No. 6,762,461). This rejection is traversed. Claim 4 depends from claim 1 and should be allowed for at least the same reasons described above. Applicants do not concede the correctness of this rejection.

Claim 5 is rejected as being unpatentable over Morikawa in view of Yoshimizu and further in view of Chen (US Patent Application No. 10/272,061). This rejection is traversed. Claim 5 depends from claim 1 and should be allowed for at least the same reasons described above. Applicants do not concede the correctness of this rejection.

Conclusion:

Applicants respectfully assert claims 1 and 3-5 are in condition for allowance. If a telephone conference would be helpful in resolving any issues concerning this communication, please contact Applicants' primary attorney-of record, Douglas P. Mueller (Reg. No. 30,300), at (612) 455-3804.

Respectfully submitted,

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